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DESIGNING A NEW REVERSIBLE ADDER/SUBTRACTOR CIRCUIT FOR LOW POWER ALU APPLICATION

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ABSTRACT

Today, low power loss systems are among the great focus of researchers. Fast and efficient processing systems are in greater demands of this period. In recent years, a huge amount of importance has been given to reversible circuits. The reversible design approach is directed towards the need for the efficient electronic system. It is one of the most important issues at the present time and has many applications such as low power CMOS, nanotechnology, quantum computing, digital signal processing etc. Arithmetic and logic circuits are considered as the important design of any digital calculating systems. In this paper, 4-bit reversible ALU using new reversible Full adder/subtractor is proposed. The proposed design is compared with a existing design in terms of quantum cost, constant input, garbage output and gate count.

KEYWORDS: Reversible Gates, Garbage, Quantum Cost, Reversible Computing, Ternary Logic & Ternary Reversible Adder/Subtractor

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Original Article

1. INTRODUCTION

As technology is advancing we are building more and more portable devices by integrating more numbers of devices. Earlier, digital logic gates were the only available design units for the construction of sequential/combinational circuits. These logic gates generate power loss due to heat generated through bit loss. Therefore, energy dissipation is one amongst the key problem in present-day technology. Energy dissipation occurs due to information loss in high technology circuits and systems which are constructed using irreversible circuits was demonstrated by R. Landauer in the year 1960. According to the Landauer's principle, the loss of one bit of information lost will dissipate kT*ln2 joules of energy where, k is Boltzmann's constant ($k=1.38x10^{-23}$), T is absolute temperature in Kelvin. The basic combinable circuits dissipate heat for every bit of information lost throughout the operation. This can be as a result of the second law of thermodynamics, information once lost cannot be recovered by any methods. In 1973, Bennet showed that to avoid kTln2 joules of energy dissipation in every circuit it should be designed from reversible circuits. According to Moores law, the numbers of transistors will double each 18 months. Reversible circuits are considered the circuits that do not lose information. The foremost necessary application of reversible logic is in quantum computers. A quantum computer is considered as a quantum network composed of quantum logic gates. Its application is within the areas like DNA computing, quantum computing, nanotechnology and Low Power CMOS style. Reversible computing is performed only if the system includes reversible gates. It supports the tactic of running the system each forward and backward i. e. computation can generate input from the output and would possibly stop and attend any point within the computation.

A gate/circuit is said to be reversible if:

- Input vector is unambiguously recovered from the output vector.
- A one-to-one mapping between input and output.

The main challenge of designing a reversible design is to chop back the amount of gates, garbage outputs, constant inputs, and quantum values/cost.

Reversibility implies that no information can ever be lost, therefore it is merely recovered within the early stage by computing backward or un-computing the results. This is logical reversibility. Physical reversibility can be a technique that dissipates no energy to heat. Completely excellent physical changeableness is dead impossible. Computing systems give off heat once the voltage level modification from positive to negative i. e. from zero to one. Most of the energy required needs to make that modification is given off within the kind of heat. Rather than dynamic voltage to new levels, reversible circuit's elements will bit by bit move charge from one node to consecutive. Throughout this technique, one can expect to lose a minimum amount of energy on each transition. Reversible computing powerfully affects digital logic style. It will impact instruction sets and high-level programming language. Eventually, these have to be compelled to be reversible to provide optimum efficiency.

1.1 Fundamental of Reversible Design

Reversible design approach aims to design any digital circuit with reversible design entities to induce lossless digital systems.

1.1.1 Reversible Digital Gate

Reversible logic gates are considered as the basic design units for the reversible circuit.

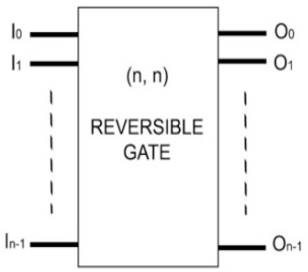


Figure 1: (nXn) Size Reversible Gate

As shown above, a reversible gate is given as (n x n) size logic gate with the subsequent characteristics:

- Equal number of input and output signals.
- One to one mapping between signals.
- No fan out.
- Output combination at any time are often properly regenerate applied input combination.
- For total n possible input combination, any output bit is high for an n/2 number of times.

1.1.2 Garbage Outputs

The garbage outputs within the design embody a logic function that isn't used as the outputs. According to the fact that in reversible circuits the number of inputs and outputs should be the same, garbage outputs are added to maintain the reversibility in the circuits. In reversible binary circuits, the values of garbage outputs are equal to zero or one, while in reversible ternary circuit, the values can be zero, one or 2.

1.1.3 Constant Input

The constant input refers to the number of inputs that should be constant at zero or one so as to realize the required reversible logic function.

1.1.4 Quantum Cost

It is the cost/value of the circuit in terms of the cost/value of a primitive gate. It is calculated by counting the quantity of primitive reversible logic gates (1*1 or 2*2) used to design a circuit. The quantum cost/value is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of 1*1 gate is zero and that of any 2*2 gate is the same, which is one.

2. REVERSIBLE GATES

Reversible logic is gaining importance in areas of CMOS style because of its low power dissipation. The basic gates like AND, OR, XOR are all irreversible gates. Consider AND gate, it consists of two inputs and one output. Thus, one bit of information is lost each time computation is carried out. According to the truth table of AND gate, there are three inputs (1, 0), (0, 1) and (0, 0) that corresponds to output 0. Thus, it is impossible to determine a unique input that results in output zero. So to make a gate reversible the input and output lines are added so that one to one mapping exists between the input and output. This will prevents the loss of information which is the main reason for power dissipation in irreversible circuits. The input that is added to an (m x n) function to make it reversible is known as constant input (CI). All the outputs of reversible circuits needn't be utilized within the circuits. Those outputs that aren't utilized in circuits is termed as garbage output (GO). The amount of garbage output for a specific reversible gate is not fixed. The 2 main constraints of reversible logic design are:

- Fan out not allowed
- Feedback or loops not allowed.

2.1 Basic Reversible Gates

Some of the main reversible gates are:

2.1.1 NOT Gate

The simplest Reversible gate is NOT gate and is a 1*1 gate with zero Quantum Cost. The gate has one input and one output i. e. P=A'. The NOT gate and its Quantum implementation are shown below:

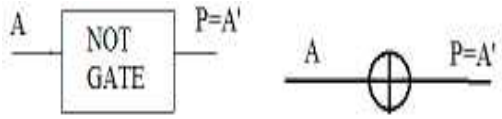


Figure 2: NOT Gate

2.1.2 Feynman Gate (FMG)

It is a 2*2 logic reversible gate with two inputs and two outputs. Feynman gate is also known as Controlled-NOT (CNOT) gate. It is also used for copying the required outputs. Also known as copying gate. Its quantum cost is one. CNOT is described as: P=A, Q=A^B. The Feynman gate and its Quantum implementation are shown below:

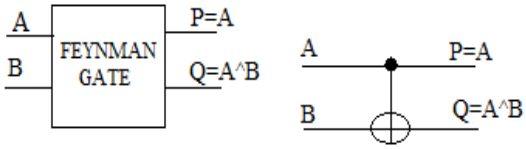


Figure 3: Feynman Gate

2.1.3 Fredkin Gate (FRG)

It is a 3 inputs and 3 outputs (3*3) reversible gate. Its quantum cost is 5. FRG is described as: P=A, Q=A'B+AC, R=AB+A'C. The Fredkin gate and its Quantum implementation are shown below:

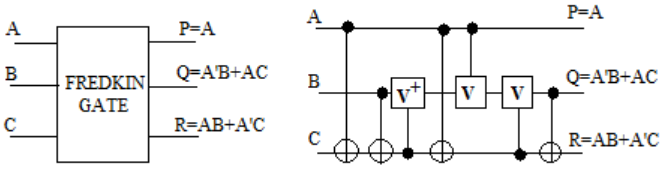


Figure 4: Fredkin Gate

2.1.4 Toffoli Gate

Toffoli gate is one of the most popular Reversible gates. It is a 3*3 gate having 3 inputs and 3 outputs. Its Quantum cost is 5. Toffoli gate is described as: P=A, Q=B, R=AB^C. The Toffoli gate and its Quantum implementation are shown below:

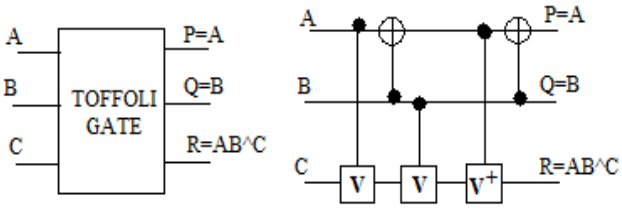


Figure 5: Toffoli Gate

2.1.5 Peres Gate

It is a 3*3 logic reversible gate. Its Quantum cost is 4. It is described as: P=A, Q=A^B, R=AB^C. The Peres gate and its Quantum implementation are shown below:

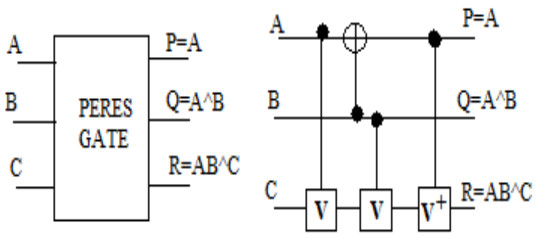


Figure 6: Peres Gate

2.1.6 New Gate

It is a 3*3 gate with 3 inputs and 3 outputs. Its Quantum cost is 11. It is described as: P=A, Q=AB^C, R=A'C'^B'. The New gate and its Quantum implementation are shown below:

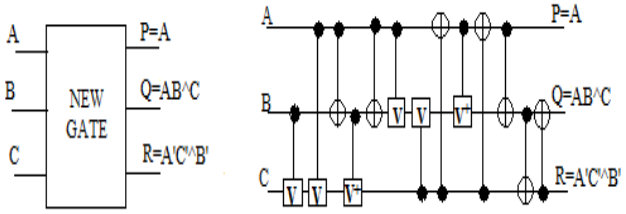


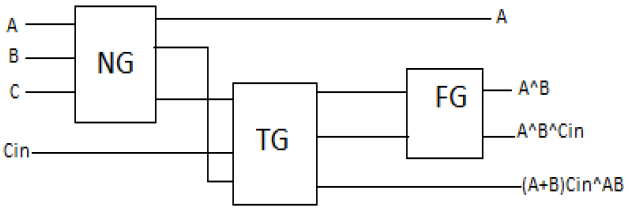
Figure 7: New Gate

3. PROPOSED FRAMEWORK

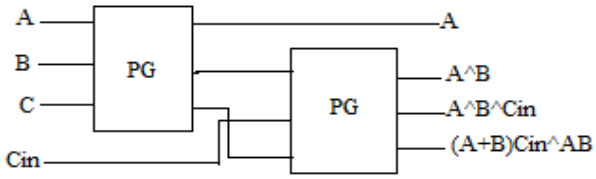
An ALU is a data processing component and a crucial component of a microprocessor and also is the core element of central processing unit. It is the main part of the instruction execution process of every computer. Different forms of computers have different ALUs. However, all of the ALUs contain arithmetic unit and logic unit, which is the fundamental structures. An ALU is a multi-functional design that conditionally performs one of several possible functions on two operands A and B depending on a selection input. Arithmetic operations contains addition, minus, while logical operations contain NOT, OR, AND, XOR and so on. All the above operations can be obtained by using reversible logic gates, through which energy consumption can be avoided.

Design of Full Adder/Subtractor Circuits

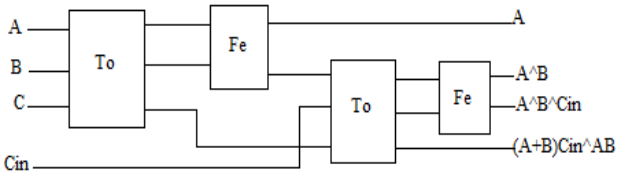
- Proposed Full adder first:



- Proposed Full adder second:



- Proposed Full adder third:



C is the constant value so it is kept as C=0 for full adder or C=1 for full subtractor.

Comparison between 1st, 2nd and 3rd full adder is shown below:

Table

Full Adders	Power
Conventional Full Adder	0.1838 uW
First Reversible Full Adder	9.6352e-02 uW
Second Reversible Full Adder	0.3104 uW
Third Reversible Full Adder	0.4387 uW

An ALU is based on reversible logic gates containing the reversible control unit and a reversible full adder. In this we have designed a 4-bit reversible ALU. The main part of the ALU is the adder/subtractor. It is used to obtain different types of the ALU operation.

- **Proposed Design**

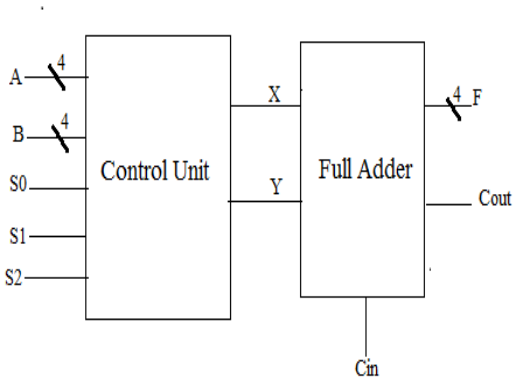


Figure 8.1: Block Diagram of 4-bit Reversible ALU

The control unit processes the input operands A and B under the control of three select lines S2, S1 and S0 along with Cin. C=0 and D=1. Cin selects fifteen operations and S distinguishes between Arithmetic and Logic operations. It has 2 constant inputs and 4 garbage outputs.

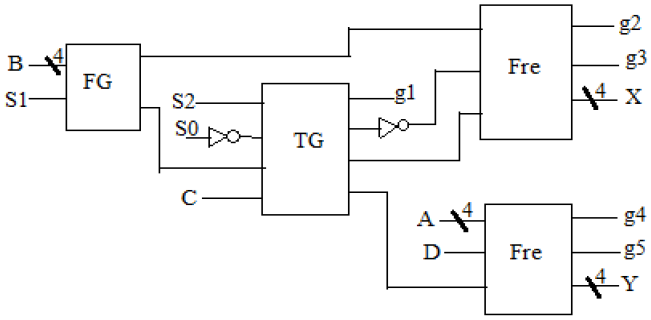


Figure 8.2: Block Diagram of Control Unit

The 1st reversible full adder is used in the ALU. It has inputs A, B and Cin and outputs S and Cout. It acts as a full adder by giving C=0 as constant value and full subtractor by giving C=1 as a constant value.

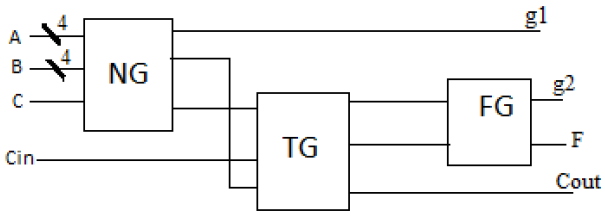


Figure 8.3: 1st Full Adder Gate

Function select				ALU Output	Adder input		Function
S_2	S_1	S_0	C_{in}		X_i	Y_i	
0	0	0	0	A_i	A_i	0	Transfer A
0	0	0	1	A_i+1	A_i	0	Increment A
0	0	1	0	A_i+B_i	A_i	B_i	Addition
0	0	1	1	A_i+B_i+1	A_i	B_i	Addition with carry
0	1	0	0	A_i+B_i-1	A_i	$\overline{B}i$	Subtraction with borrow
0	1	0	1	A_i-B_i	A_i	$\overline{B}i$	Subtraction
0	1	1	0	A_i-1	A_i	1	Decrement A
0	1	1	1	A_i	A_i	1	Transfer A
1	0	0	0	$A_i \vee B_i$	$A_i \vee B_i$	0	OR
1	0	0	1	$\overline{Ai \vee Bi}$	$A_i \vee B_i$	0	NOR
1	0	1	0	$\overline{Ai}$	A_i	1	Complement A
1	0	1	1	$A_i \wedge B_i$	$A_i \wedge \overline{B}i$	$\overline{B}i$	AND
1	1	0	0	$\overline{Ai \wedge Bi}$	$A_i \wedge \overline{B}i$	$\overline{B}i$	NAND
1	1	0	1	$A_i \oplus B_i$	A_i	B_i	EXOR
1	1	1	0	$\overline{A_i \oplus B_i}$	A_i	B_i	EXNOR

Figure 8.4: Arithmetic and Logical Operations

- **Existing Design**

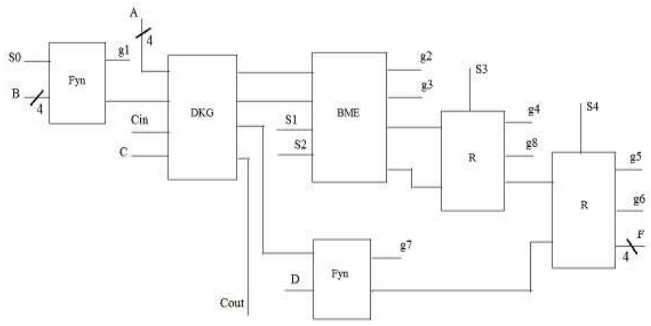


Figure 8.5: Block Diagram of 4-bit Reversible Gate ALU

4. SIMULATION AND RESULT

The 4-bit reversible ALU architecture presented and explained in the previous section is synthesized and simulated on Model Sim-Altera 10.1 tool. The simulation waveforms 4-bit reversible ALU is shown in figure 9.1 and simulation waveform of existing 4-bit reversible ALU is shown in figure 9.2.

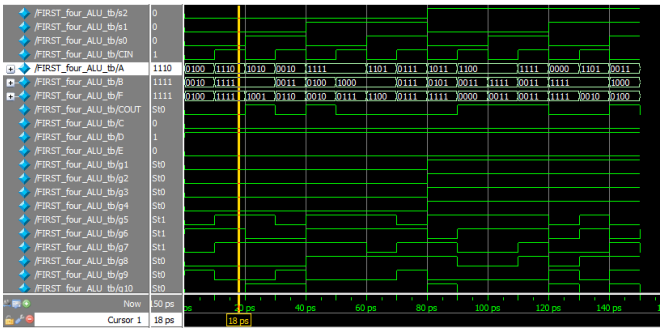


Figure 9.1: Simulation Waveform of Proposed Reversible 4-bit ALU

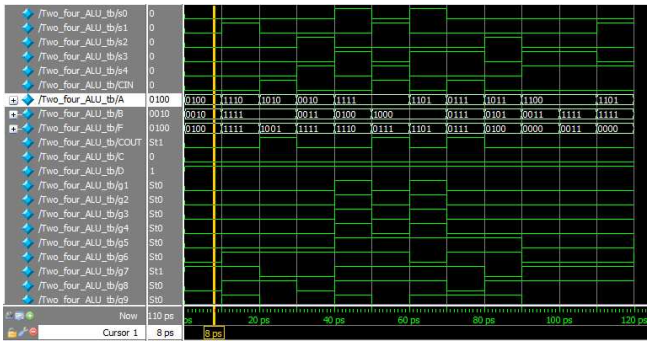


Figure 9.2: Simulation waveform of Existing Reversible 4-bit ALU

Table 9.3 show the performance comparison of the 4-bit existing ALU design with the proposed 4-bit reversible ALU designs. For comparison, constant input, gate count, quantum cost and garbage output are considered as the performance matrices.

Table 9.3: Performance Parameter Table

Parameters	Proposed Design	Existing Design
Power	6.6217 uW	10.7754 uW
Constant inputs	12	8
Garbage outputs	28	32
Gate count	20	24
Quantum cost	132	88

5. CONCLUSIONS

In this paper, 4-bit reversible ALU i. e. reversible control unit and reversible full adder unit has been implemented on ModelSim-Altera 10.1 tool. We have compared this proposed design with the existing design in terms of reversible gates used, Garbage outputs, Quantum cost, constant inputs. ALU using reversible control unit has great improvement over existing design. Reversible logic has several applications, like low power CMOS, quantum computing, nanotechnology, optical computing, digital signal process, communication and computer graphics, etc. Reversible computing has a lot of importance in reducing the quality of the digital circuits. In future we can style, complete/complex reversible design with

the assistance of proposed designs.

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